

## IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of:

Shota KITAMURA of Kanagawa-ken, Japan and Seiji YAMADA  
of Tokyo-to, Japan

Serial No: not assigned

Filed: September 9, 1999

For: NONVOLATILE SEMICONDUCTOR MEMORY DEVICE  
AND ITS MANUFACTURING METHOD

Box PATENT APPLICATION

Assistant Commissioner for Patents

Washington, D.C. 20231

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Transmitted herewith for filing is the patent application identified above.

- ☒ 14 sheet(s) of drawings (☒ formal ☐ informal) is(are) enclosed.
- ☒ 16 page(s) of specification and 1 page(s) of abstract of the invention are enclosed.
- ☐ An assignment of the invention to KABUSHIKI KAISHA TOSHIBA ☐ is enclosed ☒ will follow.
- ☐ An associate power of attorney ☐ is enclosed ☐ will follow.
- ☐ A verified statement to establish small entity status under 37 C.F.R. §§ 1.9 & 1.27 is enclosed.
- ☐ Declaration and Power of Attorney ☐ is enclosed ☒ will follow.
- ☐ A certified copy of Japanese Patent Application No. 255619/1998 filed September 9, 1998 from which priority is claimed under 35 U.S.C. § 119 will follow.
- ☐ IDS enclosed (☐ with references).
- ☐ Preliminary Amendment is enclosed.

## CALCULATION OF FEES

CALCULATION OF FEES								
ITEM		TOTAL NO. OF CLAIMS		NO. OF CLAIMS OVER BASE	LG/SM \$ ENTITY FEE		\$ AMOUNT	\$ FEE
A	TOTAL CLAIMS FEE	15	-20	0	LG=\$18 SM=\$9	\$18	0	
B	INDEPENDENT CLAIMS FEE*	2	-3	0	LG=\$78 SM=\$39	\$78	0	
C	SUBTOTAL - ADDITIONAL CLAIMS FEE (ADD FINAL COLUMN IN LINES A + B)							\$ 0
D	MULTIPLE-DEPENDENT CLAIMS FEE				LARGE ENTITY FEE = \$260 SMALL ENTITY FEE = \$130			\$ 0
E	BASIC FEE				LARGE ENTITY FEE = \$760 SMALL ENTITY FEE = \$380			\$ 760
F	TOTAL FILING FEE (ADD TOTALS FOR LINES C, D, AND E)							\$ 760
G	ASSIGNMENT RECORDING FEE						\$ 40	\$ 40
	*LIST INDEPENDENT CLAIMS 1 and 8							

- ☐ A check in the amount of \$ 0 to cover the filing fee is enclosed.
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Respectfully submitted,  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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I hereby certify that

- ☒ two copies of a letter of transmittal
- ☒ patent application ( 16 page(s) of specification; 15 claim(s); 1 page(s) of abstract
- ☒ 14 sheet(s) of formal drawings
- ☐ assignment of the invention to KABUSHIKI KAISHA TOSHIBA
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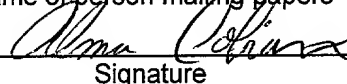
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NONVOLATILE SEMICONDUCTOR MEMORY DEVICE  
AND ITS MANUFACTURING METHOD

BACKGROUND OF THE INVENTION

5 Field of the Invention

This invention relates to a nonvolatile semiconductor memory device, such as EEPROM, and its manufacturing method.

Background Art

10 A nonvolatile semiconductor memory device is made of a plurality of memory transistors (memory cells) each having a gate, source and drain diffusion layers to perform nonvolatile storage of an electric charge in response to a data. Representative one of electrically rewritable EEPROM-type memory cells is introduced below. This is a MOS transistor including a floating  
15 gate made on a semiconductor substrate via a tunneling insulating film as a first gate insulating film, and a control gate stacked thereon via a second gate insulating film. Each floating gate is independently formed for each memory cell to function as a charge storage layer. The control gate is common to a plurality  
20 of memory cells to function as a word line.

From the viewpoint of connection of memory cells of EEPROM, there are the following two representative types of memory cells. One of them is NOR-type cells in which drains of a plurality of memory transistors are connected in parallel to a single bit line.  
25 The other is NAND-type cells in which adjacent ones of memory cells commonly share a source diffusion layer or a drain diffusion layer, then a plurality of transistors are connected in series, and the drain diffusion layer at one end thereof is connected to a bit line.

30 When integrating memory cells of EEPROM in a micro pitch, side wall insulating films (protective side walls) are selectively made on opposite side walls of the gate of each cell for the protective purpose. Typical side wall insulating film is a silicon oxide ( $\text{SiO}_2$ ) film made by CVD. A substrate having  
35 memory cells thereon has formed wiring layers such as bit lines via one or more inter-layer insulating films. Typically used as the inter-layer insulating film is a silicon oxide film made by

CVD. Since the inter-layer insulating film is thick, when contact holes, etc. are made, there is the need for increasing the processing margin while preventing excessive etching of the base layer.

5           Therefore, when a CVD silicon oxide film is used as the inter-layer insulating film, it is desirable to make a silicon nitride film on the base layer to behave as an etching stopper. In this case, the silicon nitride film results in preventing that the side-wall insulating films in form of silicon oxide films  
10       provided on opposite side walls of a memory cell are etched. As a result, in a memory cell array including memory cells in a micro pitch, micro contact can be made reliably.

          There is a report, however, that memory cells deteriorate in reliability when using silicon oxide films as both side wall  
15       insulating films (protective side walls) and the inter-layer insulating film of each memory cell and forming a silicon nitride film as the base layer of the inter-layer insulating film. That is, while data reads are performed, some electrons are injected into floating gates of erased memory cells to vary threshold  
20       values thereof (read disturb). This is currently considered to be caused by the phenomenon that hydrogen generated during deposition of the silicon nitride film undesirably spreads into the gate insulating films (particularly, tunneling oxide film) of each memory cell.

25           In the case where a metal silicide film is selective formed on surfaces of the gate, source and drain diffusion layers for the purpose of reducing the resistance, a restriction is imposed to a subsequent high-temperature annealing process. Therefore, plasma CVD enabling deposition at a low temperature is preferably  
30       used to stack or deposit the silicon nitride film. However, a silicon nitride film obtained by plasma CVD is more liable to generate hydrogen than a silicon nitride film obtained by low-pressure CVD. Therefore, the above-indicated deterioration of memory cells in reliability is serious especially when the  
35       silicon nitride film is stacked or deposited by plasma CVD.

          In the case where low-pressure CVD is used for stacking or depositing the silicon nitride film, deterioration of memory

cells is less than those by plasma CVD. However, prevention of deterioration in reliability still remains unsatisfactory. A reason thereof is as set forth below. Silicon nitride films are dense films. Therefore, both of the side wall insulating films of a memory cell are made of silicon films, impurities contained in the silicon oxide films probably get to be confined in the memory cell area by the silicon nitride films. That is, impurities contained in the silicon oxide films on opposite side walls might lose their ways of escape and adversely behave to deteriorate the reliability of the memory cell.

#### SUMMARY OF THE INVENTION

It is therefore an object of the invention to provide a nonvolatile semiconductor memory device realizing a high reliability, and its manufacturing method.

According to the invention, there is provided a nonvolatile semiconductor memory device comprising:

- a semiconductor substrate;
- memory transistors formed on the semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data;
- protective side walls in form of first silicon nitride films formed by low-pressure CVD and maintained on side walls of gates of each memory transistor;
- a second silicon nitride film covering surfaces of the gate, surface of a source diffusion layer, surface of a drain diffusion layer and surfaces of the protective side walls of each memory transistor; and
- a wiring layer formed on the second silicon nitride film via an inter-layer insulating film containing silicon oxide as its major component.

According to the invention, there is further provided a method for manufacturing a nonvolatile semiconductor memory device comprising:

- a first step of forming in a semiconductor substrate memory transistors for performing nonvolatile storage of an electric charge in accordance with data;

a second step of stacking a first silicon nitride film by low-pressure CVD to cover the memory transistors and selectively maintaining the first silicon nitride film as protective side walls on side walls of gates of each memory transistor;

5 a third step of stacking a second silicon nitride film to cover surfaces of gates, a surface of a source diffusion layer, a surface of a drain diffusion layer and the protective side walls; and

10 a fourth step of forming a wiring layer above the second silicon nitride film via an inter-layer insulating film including a silicon oxide film as its major component.

The invention uses a dense first silicon nitride film made by low-pressure CVD, instead of a silicon oxide film, as side-wall  
15 protective films of each memory transistor. therefore, even when the second silicon nitride film is made by plasma CVD, diffusion of hydrogen, or the like, into the memory cell can be prevented, and the memory transistor can be reliably prevented from deteriorating in reliability.

20 In the silicon nitride film by low-pressure CVD, even if containing impurities, the movement of impurities is small as compared with silicon oxide films by low-pressure CVD. Therefore, even when the second silicon nitride film covers the memory transistor area, deterioration in reliability caused by  
25 impurities spreading from the side walls, i.e., the gate insulating film, is alleviated. Therefore, even when the second silicon nitride film is stacked by low-pressure CVD, deterioration in reliability can be alleviated as compared with the conventional type using silicon oxide films as side-wall  
30 insulating films.

Furthermore, according to the invention, since the second silicon nitride film covers the memory transistor area to form the inter-layer insulating film including the silicon oxide film as its major component, in the etching process for making contact  
35 holes, etc. in the inter-layer insulating film, the silicon nitride film as its base layer behaves as an etching stopper. Therefore, when the inter-layer insulating film is over-etched

to make a processing margin, or there is a deviation in fitting a mask for making contact holes, useless etching of the underlying silicon substrate and the insulating film for separating devices can be prevented.

5

#### BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a layout of a memory cell array of EEPROM according to an embodiment of the invention;

10 Figs. 2A and 2B are cross-sectional views taken along the A-A' line and B-B' line in Fig. 1;

Figs. 3A and 3B are cross-sectional views taken along the C-C' line and D-D' line of Fig. 1;

15 Figs. 4A and 4B are cross-sectional views corresponding to Figs. 2A and 2B, showing different steps of a process for making gates of the same memory cell array;

Figs. 5A and 5B are cross-sectional views similarly showing different steps of a process for making source and drain diffusion layers;

20 Figs. 6A and 6B are cross-sectional views similarly showing different steps of a process for stacking the first silicon nitride film;

Figs. 7A and 7B are cross-sectional views similarly showing different steps of a process for maintaining the first silicon nitride film as side wall insulating films (side walls);

25 Figs. 8A and 8B are cross-sectional views similarly showing different steps of a process for making a titanium silicide film in memory cells;

30 Figs. 9A and 9B are cross-sectional views similarly showing different steps of a process for stacking a silicon oxide film as the first layer of the inter-layer insulating film;

Figs. 10A and 10B are cross-sectional views similarly showing different steps of a process for burying a common source line in the silicon oxide film;

35 Figs. 11a and 11B are cross-sectional views similarly showing different steps of a process for stacking a silicon oxide film as the second layer of the inter-layer insulating film to form a bit line;



Fig. 12 is a cross-sectional view showing a structure of a MOS transistor as a peripheral circuit;

Fig. 13 is a cross-sectional view taken along the D-D' line of Fig. 1, under the presence of an offset in bit line contact holes;

Fig. 14 is a cross-sectional view corresponding to Fig. 13 without the use of the silicon nitride film; and

Fig. 15 is a diagram showing data of a reliability test of the memory cell according to the embodiment of the invention, together with those of comparative examples.

#### DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Explained below is an embodiment of the invention with reference to the drawings.

Fig. 1 shows a layout of a central area of a memory cell array having a NOR-type EEPROM structure according to an embodiment of the invention. Figs. 2A and 2B are cross-sectional views taken along the A-A' line and B-B' line of Fig. 1. Figs. 3A and 3B are cross-sectional views taken along the C-C' line and D-D' line of Fig. 1.

A memory transistor (memory cell) includes a floating gate 4 formed in a region of a p-type silicon substrate (or p-type well) 1 sandwiched by two device-separation insulating films 2, 2 via a first gate insulating film (tunneling oxide film) 3, and a control gate 6 formed on the floating gate 4 via a second gate insulating film 5. An n<sup>+</sup>-type source diffusion layer 7a and a drain diffusion layer 7b are further provided in self alignment with the control gate 6.

The floating gate 4 is made of a first polycrystalline silicon film, and it is independently provided for each memory cell. Each control gate 6 is made of a second polycrystalline silicon film, and it transversely extends over a plurality of memory cells in an elongated pattern to form a word line. A separation groove between every two adjacent floating gates 4, 4 aligned along the word line is processed and formed before the second polycrystalline silicon film is formed to make the control gates 5, 6. In the direction along the bit line, the floating

gates 4, 4 are separated by patterning the first polycrystalline silicon film simultaneously upon stacking the second polycrystalline silicon film and patterning the control gates 6, 6.

5 In the embodiment shown here, the  $n^+$ -type source and drain diffusion layers 7a and 7b are formed in a  $p^-$ -type layer 8 made simultaneously with these  $n^+$ -type source and drain diffusion layers 7a, 7b. On surfaces of the source and drain diffusion layers 7a, 7b and the control gate 6, a titanium silicide film  
10 9 is formed to reduce the resistance.

On opposite side walls of the gates in each memory cell, first silicon nitride film 10 are formed by low-pressure CVD. Then, a second silicon nitride film 11 is formed to cover surfaces of the control gate 6, silicon nitride films 10 on the side walls,  
15 source and drain diffusion layers 7a and 7b. Further formed thereon is a silicon oxide film 12 (12a, 12b) by CVD as an inter-layer insulting film. The silicon oxide film 12 may be any film including a silicon oxide  $\text{SiO}_2$  film as its major component. For example, a BSG film or a BPSG film is acceptable. The second  
20 silicon nitride film 11 is a nitride film by plasma CVD, in this embodiment.

The first-layer silicon oxide film 12a is smoothed along its surface, and wiring grooves 20, 20 are made therein. In these wiring grooves 20, common source lines 13, 13 are embedded for  
25 connection to the source diffusion layer 7a of the memory cell. Each common source line 13 extends in parallel to the control gate 6 (word line) as shown by broken lines in Fig. 1 to work for a plurality of memory cells. Contact holes 21, 21 are made to pass through the first-layer and second-layer silicon oxide  
30 films 12a and 12b. Bit lines 14, 14 are made to extend across the word lines. The bit line 14 partly extend through the contact holes 21, 21 to get into contact with the drain diffusion layer 7b, 7b of the memory cells.

Figs. 4A, 4B through Figs. 10A and 10B are cross-sectional  
35 views corresponding to Figs. 2a and 2B, showing different steps of a manufacturing process of the same memory cell array. Referring to these drawings, a specific manufacturing process

is explained below.

As shown in Figs. 4A and 4B, device-separation insulating films 2, 2 are formed in the silicon substrate 1. The device-separation insulating films 2, 2 are made by, for example, STI (shallow trench isolation) in which, after shallow trenches are made on the substrate 1, a silicon oxide film is stacked by CVD and then smoothed to be embedded therein. Alternatively, the device separation oxide films 2, 2 may be made by LOCOS.

After that, the floating gates 4, 4 are formed in respective device sites via the first gate insulating film 3 by processing the first-layer polycrystalline silicon film 12a. Furthermore, the control gates 6, 6 are formed therein via the second gate insulating films 5, 5 by processing the second-layer polycrystalline silicon film. In the first-layer polycrystalline silicon film, separation grooves are made in their device-separation regions by RIE. Thereafter, simultaneously with etching the second polycrystalline silicon film by RIE, the first polycrystalline silicon film is etched. As a result, each control gate 6 and each floating gate 4 can be patterned while matching their ends in the bit line direction with each other.

After that, as shown in Figs. 5a and 5B, secondary oxidation is conducted to cover the control gate 6 and the exposed surface of the silicon substrate 1 with an oxide film 31 as thick as 10 nm approximately. The oxide film 31 behaves as a buffer during ion implantation. Thereafter, a p-type impurity and an n-type impurity are ion-implanted to form the n<sup>+</sup>-type source and drain diffusion layers 7a, 7b surrounded by the p<sup>-</sup>-type layer 8.

Subsequently, as shown in Figs. 6A and 6B, a silicon oxide film 32 as thin as 20 nm is stacked or deposited by CVD using TEOS (tetraethyloxysilane) as a source material. Next, a silicon nitride film 10, 150 nm thick, approximately, is stacked by low-pressure CVD. The silicon oxide film 32 functions as a stopper mask during etching of the silicon nitride film 10. Thereafter, the silicon nitride film 10 is etched by RIE. As a result, as shown in figs. 7A and 7B, the silicon nitride film 10 is selectively maintained as protective side walls solely on

side walls of both gates of each memory cell.

After that, using the silicon nitride film 10 as a mask, the silicon oxide films 32 and 31 are etched to expose surfaces of the control gate 6, and source drain diffusion layers 7a, 7b.

5 Then, a titanium (Ti) film is deposited and annealed. As a result, as shown in Figs. 8A and 8B, titanium silicide films 9, 9 are selectively formed on surfaces of the control gate 6 and source drain diffusion layers 7a, 7b. The titanium film not contributing to the chemical interaction is removed thereafter.

10 After that, as shown in Figs. 9A and 9B, after the silicon nitride film 11 as thick as approximately 50 nm is stacked by plasma CVD, the first-layer silicon oxide film 12a as the inter-layer insulating film is stacked by low-pressure CVD. The silicon nitride film 11 is a base layer of the inter-layer  
15 insulating film. It contacts the surfaces of the control gate 6, source and drain diffusion layers 7a, 7b and silicon nitride films 10 as the side walls of each memory cell to cover the memory cell, and also covers the device separation regions. The surface of the silicon oxide film 12a is smoothed by CMP processing. Then,  
20 as shown in Fig. 10A and 10B, wiring grooves 20, 20 are formed in the silicon oxide film 12a by RIE. Each groove 20 is continuous over the source diffusion layers 7a, 7a. A common source line 13 is buried in each wiring groove 20.

When the silicon oxide film 12a is etched by RIE, the  
25 silicon nitride film 11 behaves as an etching stopper under a gas condition ensuring a large ratio in etching selectively relative to the silicon nitride film 11. Therefore, by conducting over-etching, the silicon oxide film 12 can be etched reliably. Although each wiring groove 20 is formed to also extend  
30 into the device separation region as shown in Fig. 10B, the silicon nitride film 11 behaves as a stopper also in the device separation region, and prevents the device separation insulating film 2 being etched undesirably. Additionally, even if a deviation exists in location of the mask for the wiring groove 20, the silicon nitride  
35 film 11 behaves as a mask, and prevents the device separation insulating film 2 from being etched uselessly. The silicon nitride film 11 exposed into the wiring groove 20 is removed later

by RIE using a different gas, and each silicide film 9 on each source diffusion layer 7a is exposed accordingly.

Next, as shown in Figs. 11A and 11B, the second-layer silicon oxide film 12b is stacked, contact holes 21, 21 are made by RIE, and bit lines 14, 14 to be connected to the drain diffusion layers 7b, 7b are made. Also in the RIE process of contact holes 21, 21 for bit lines, by employing the same conditions as used in the RIE process for making wiring grooves 20, 20 of common source lines, reliable etching is ensured by the silicon nitride film 11 behaving as a mask.

In the peripheral circuit area, at least one of a high-voltage MOS transistor supplied with a high write voltage, etc. and an ordinary low-voltage MOS transistor operative under a voltage below the source voltage VCC is formed. Fig. 12 shows a structure of the high-voltage MOS transistor and the low-voltage MOS transistor as the peripheral circuit. These MOS transistors as the peripheral circuit are made in a process separate from that of the memory cells.

A manufacturing process of the peripheral circuit MOS transistors is explained briefly. In the status shown in Figs. 5a and 5B just after the gate, source and drain of the memory cell are made in the memory cell array area, the memory cell array area is masked, a gate electrode 4 is made in the peripheral circuit area via a gate insulating film 41, and ions are implanted to form the  $n^+$ -type source and drain diffusion layers 43a, 43b. More specifically, the source and drain diffusion layers 43a, 43b are formed as an LDD structure having low-concentrated  $n^-$ -type layers 44 at lateral ends of the channels.

After that, the silicon nitride film 10 as the side wall insulating films is stacked and etched, the silicon nitride film 11 is next stacked by plasma CVD, the inter-layer insulating film 12 is next stacked, the contact holes are made, and the wiring layer is formed. These steps are different from those of the memory cell array area.

In the embodiment shown here, since the silicon nitride film 11 is formed to underlie the silicon oxide film 12a as the inter-layer insulating film, useless etching is prevented in the

etching step of the wiring grooves 20, 20 and the contact holes 21, 21. In a typical etching process, over-etching somewhat elongating the etching time is conducted, paying attention to leaving no residue of the material to be etched. In this embodiment, however, since the silicon nitride film 11 functions as a stopper, over-etching is employable, and the processing margin can be increased accordingly.

Additionally, even if resist masks for making the wiring grooves 20 and the contact holes 21 are positionally deviated or the size of the mask openings are somewhat large, the silicon nitride film 11 prevents the device separation insulating film 2 and others from being etched undesirably. This aspect is shown in Fig. 13, taking the case of the contact hole 21 for a bit line in a cross-sectional view taken along the D-D' line of Fig. 1 (that is, corresponding to the cross-sectional view of Fig. 3B). When the silicon nitride film 11 is not used, over-etching will result in etching the device separation insulating film 2 when the contact hole 21 overlaps the device separation insulating film 2 as shown in fig. 14. This will cause the bit line to be short-circuited.

Moreover, according to the embodiment, by using the silicon nitride film 10 by low-pressure CVD as the side wall insulating film of the memory cell, instead of a silicon oxide film, even when the silicon nitride film is formed by plasma CVD neat the memory cell, the reliability of the memory cells does not deteriorate. This feature is explained more specifically by using data.

Fig. 15 shows statistical data of the number of bits causing threshold voltage  $V_{th}$  of each memory cell to shift upon data read operation after data write and erase operations are repeated over 10000 times in EEPROMs according to the embodiment and comparative examples 1 through 3. In Fig. 14, the abscissa is the threshold value  $V_{th}$ , and the shifting amount increases from the initial value toward the right end. The ordinate indicates a standard declination of the bits shifting the threshold values. Comparative Example 1 (plotted by white circles) uses a silicon oxide film as the sidewall insulating film and includes no silicon

nitride film 11 by plasma CVD as used in the embodiment. Comparative Example 2 (plotted by triangles) uses a silicon nitride film by low-pressure CVD as the side wall insulating film, and includes no silicon nitride film 11 by plasma CVD as used  
5 in the embodiment.

Unlike these Comparative Examples 1 and 2, Comparative Example 3 (plotted by black points) uses a silicon oxide film as the side wall insulating film and uses a silicon nitride film 11 by plasma CVD like the embodiment. Comparative Example 3  
10 exhibits a large shift amount of threshold value as compared with Comparative Examples 1 and 2 apparently as a result of the use of the silicon nitride film 11 by plasma CVD. On the other hand, in case of the embodiment (plotted by x) using the silicon nitride film 10 as the low-pressure CVD as the side wall insulating film  
15 and additionally providing the silicon nitride film 11 by CVD, no shift in threshold value caused by the use of the silicon nitride film 11 by plasma CVD is observed, and a high reliability on the same level as Comparative Examples 1 and 2 is confirmed.

In this embodiment, a main reason of stacking the second-layer silicon nitride film 11 by plasma CVD lies in that  
20 the titanium silicide film 9 is formed in the memory cell area and it restricts later high-temperature processes. Since plasma CVD enables deposition of films under a lower temperature than that of low-pressure CVD, the titanium silicide film 9 can be  
25 prevented from deterioration.

The invention, however, is still effective also when the second-layer silicon nitride film 11 is stacked by low-pressure CVD similarly to the first-layer silicon nitride film 10 used as the side wall insulating film. When the silicon nitride film  
30 11 is stacked by low-pressure CVD, the film becomes dense, and results in confining impurities contained in the side wall insulating film. However, since the invention uses the silicon nitride film by low-pressure CVD as the side wall insulating film as well, movements of impurities in the film are small unlike  
35 the structure using a silicon oxide film, and the memory cell is less adversely affected by diffusion of impurities.

Furthermore, although the embodiment has been explained,

taking NOR-type EEPROM as an example, the invention is similarly applicable to any other nonvolatile semiconductor memory devices such as NAND EEPROM, needless to say, and EPROM, mask ROM, and so forth.

5           As described above, according to the invention, since a first silicon nitride film by low-pressure CVD is used as each side wall protective film of a memory transistor, deterioration in reliability of the memory transistor is reliably prevented even when a second silicon nitride film is made later by plasma  
10 CVD.

          Furthermore, since impurities do not move so much in the silicon nitride film by low-pressure CVD, even when the memory transistor area is covered by the second silicon nitride film, the reliability does not deteriorate so much due to impurity  
15 diffusion from side walls into the gate insulating film. Therefore, even when the second silicon nitride film is stacked by low-pressure CVD, deterioration in reliability is alleviated as compared with the conventional device using the silicon oxide film as the side wall insulating film.

20           Moreover, according to the invention, since the silicon nitride film is formed as the base layer of the inter-layer insulating film, the silicon nitride film behaves as an etching stopper in the etching process of the inter-layer insulating film for making contact holes, etc. Therefore, a large processing  
25 margin can be provided while preventing useless etching of the substrate and the device separation insulating film.



## WHAT IS CLAIMED IS:

1. A nonvolatile semiconductor memory device comprising:  
a semiconductor substrate;  
memory transistors formed on said semiconductor substrate to perform nonvolatile storage of an electric charge in accordance with data;  
protective side walls in form of first silicon nitride films formed by low-pressure CVD and maintained on side walls of gates of each said memory transistor;  
a second silicon nitride film covering surfaces of said gate, surface of a source diffusion layer, surface of a drain diffusion layer and surfaces of said protective side walls of each said memory transistor; and  
a wiring layer formed on said second silicon nitride film via an inter-layer insulating film containing silicon oxide as its major component.
2. The nonvolatile semiconductor memory device according to claim 1 wherein said each memory transistor is an electrically rewritable memory transistor including a floating gate formed on said semiconductor substrate via a first gate insulating film, and a control gate formed above said floating gate via a second gate insulating film.
3. The nonvolatile semiconductor memory device according to claim 1 wherein said second silicon nitride film is deposited by plasma CVD.
4. The nonvolatile semiconductor memory device according to claim 1 wherein said second silicon nitride film is deposited by low-pressure CVD.
5. The nonvolatile semiconductor memory device according to claim 4 wherein metal silicide films are formed on surfaces of a gate, a surface of a source diffusion layer and a surface of a drain diffusion layer of each said transistor, respectively.

6. The nonvolatile semiconductor memory device according to claim 5 wherein said drain diffusion layer connects to a bit line via said metal silicide film and said source diffusion layer connects to a common source line via said metal silicide film, respectively.

7. The nonvolatile semiconductor memory device according to claim 1 further comprising at least one of a low-voltage MOS transistor and a high-voltage MOS transistor as a peripheral circuit.

8. A method for manufacturing a nonvolatile semiconductor memory device comprising:

a first step of forming in a semiconductor substrate memory transistors for performing nonvolatile storage of an electric charge in accordance with data;

a second step of depositing a first silicon nitride film by low-pressure CVD to cover said memory transistors and selectively maintaining said first silicon nitride film as protective side walls on side walls of gates of each said memory transistor;

a third step of stacking a second silicon nitride film to cover a surface of gate, a surface of a source diffusion layer, a surface of a drain diffusion layer and said protective side walls of said memory transistor; and

a fourth step of forming a wiring layer above said second silicon nitride film via an inter-layer insulating film including a silicon oxide film as its major component.

9. The method for manufacturing a nonvolatile semiconductor memory device according to claim 8 wherein, in said third step, said second silicon nitride film is deposited by plasma CVD.

10. The method for manufacturing a nonvolatile semiconductor memory device according to claim 8 wherein, in said third step, said second silicon nitride film is deposited by low-pressure

CVD.

11. The method for manufacturing a nonvolatile semiconductor memory device according to claim 8 wherein, after selectively maintaining said first silicon nitride film as said protective side walls on said side walls of gates in said second step and before depositing said second silicon nitride film in said third step, a metal silicide film deposition step is interposed for selectively making a metal silicide film on said surfaces of a gate, said surface of the source diffusion layer, and said surface of the drain diffusion layer.

12. The method for manufacturing a nonvolatile semiconductor memory device according to claim 11 wherein an oxide film covering step for covering exposed surfaces of said semiconductor substrate and said memory transistors is interposed between said first step and said second step, and in said metal silicide film deposition step, by etching said oxide film, said surfaces of the gate, said surface of the source diffusion layer and said surface of the drain diffusion layer are exposed, and thereafter said metal silicide film is formed.

13. The method for manufacturing a nonvolatile semiconductor memory device according to claim 12 wherein said oxide film covering step includes two steps, one of which is an oxidation step by secondary oxidation and the other of which is an oxidation step by CVD.

14. The method for manufacturing a nonvolatile semiconductor memory device according to claim 11 wherein said metal silicide film is a titanium silicide film.

15. The method for manufacturing a nonvolatile semiconductor memory device according to claim 11 wherein said second to fourth steps are common to a manufacturing step of at least one of a low-voltage MOS transistor and a high-voltage MOS transistor as a peripheral circuit.

ABSTRACT OF THE DISCLOSURE

Memory cells each having a floating gate (4), control gate (6), and source and drain diffusion layers (7a, 7b) are formed on a silicon substrate (1). A silicon nitride film (10) by low-pressure CVD is maintained as side wall insulating films on side walls of the gates in each memory cell. A silicon nitride film (11) by plasma CVD is formed to cover a memory cell array, and silicon oxide films (12a, 12b) are made on the silicon nitride film (11) to form an inter-layer insulating film. A common source line (13) connected to the source diffusion layer 7a is formed to embed in the silicon oxide film (12a), and a bit line (14) connected to the drain diffusion layer (7b) is formed on the silicon oxide film (12b).

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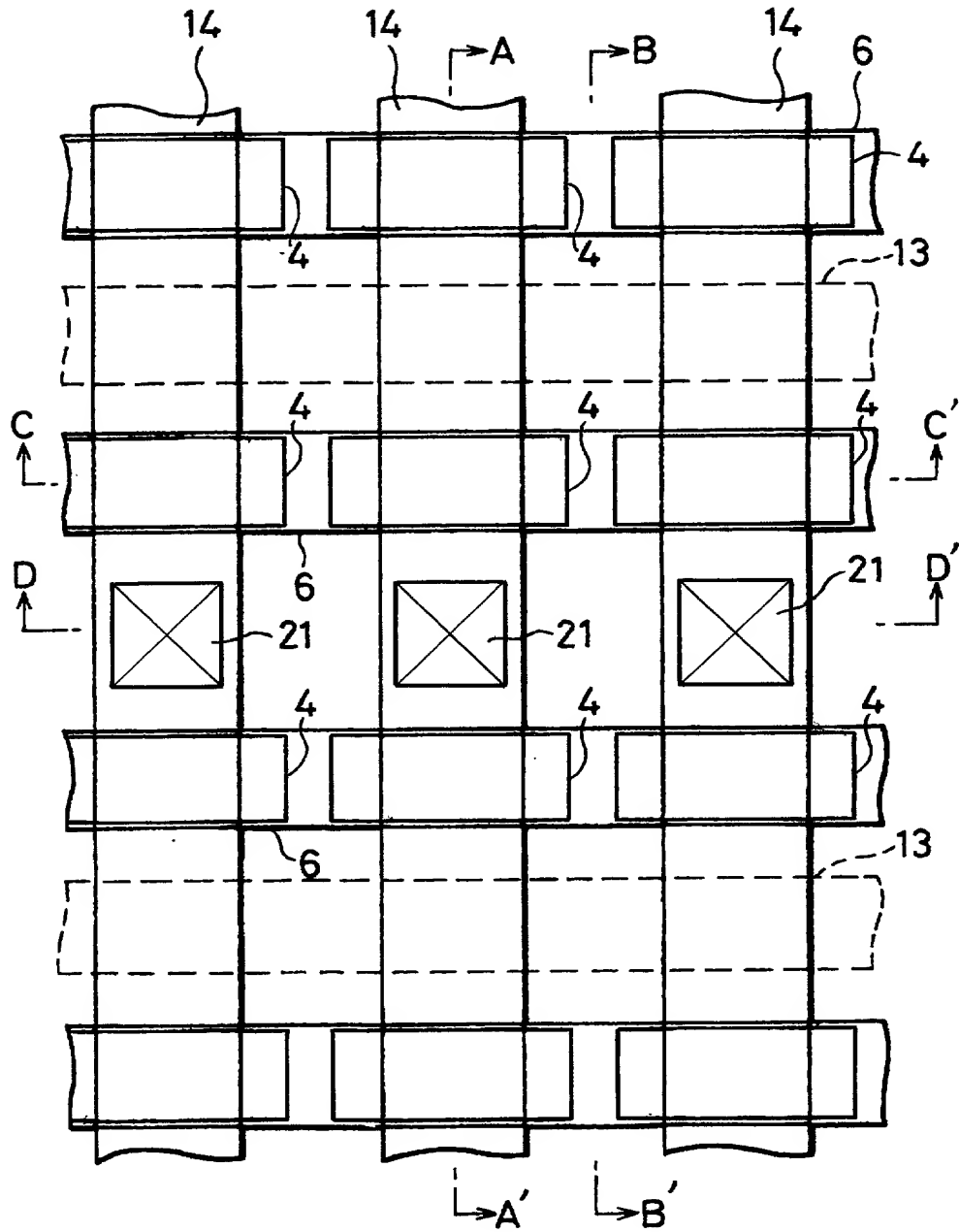


FIG. 1

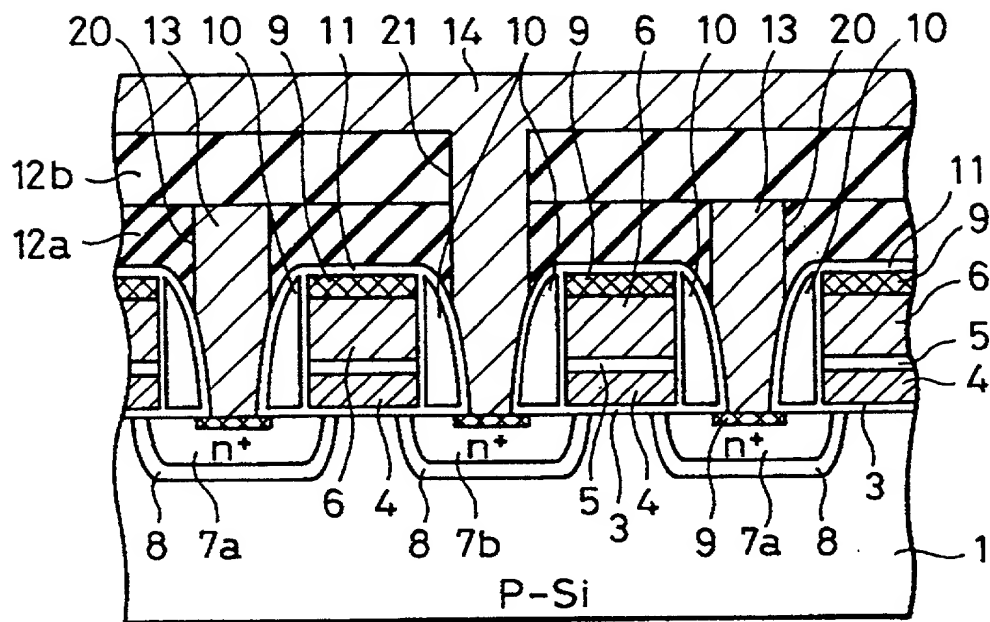


FIG. 2 (a)

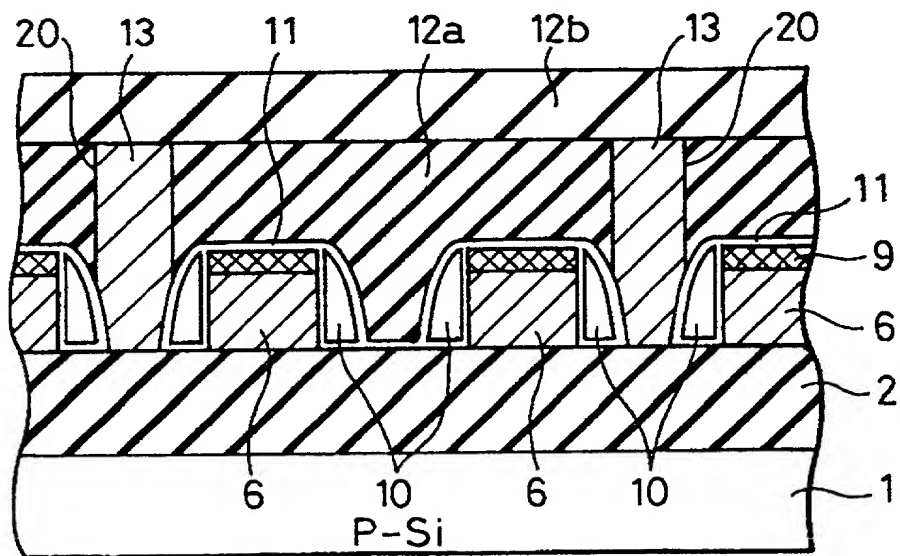


FIG. 2 (b)

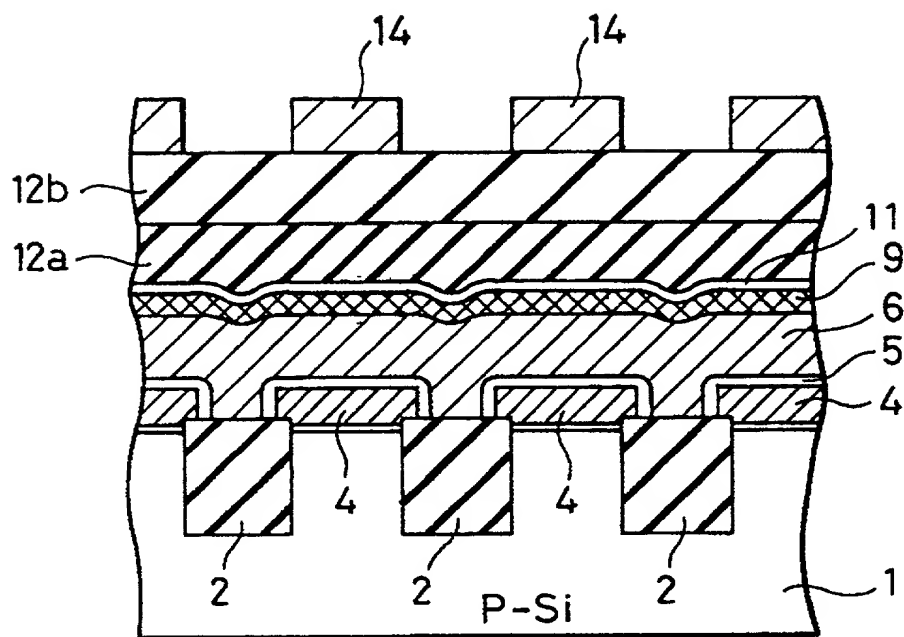


FIG. 3 (a)

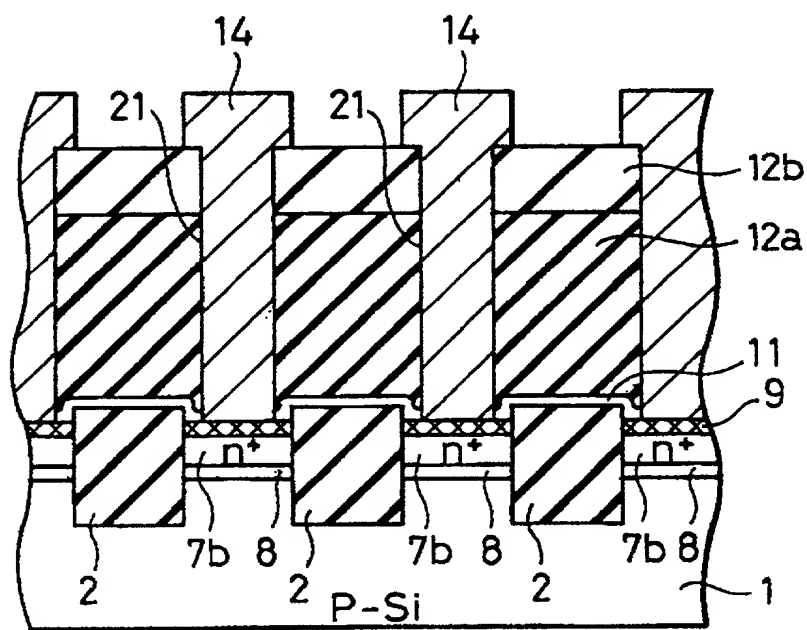


FIG. 3 (b)

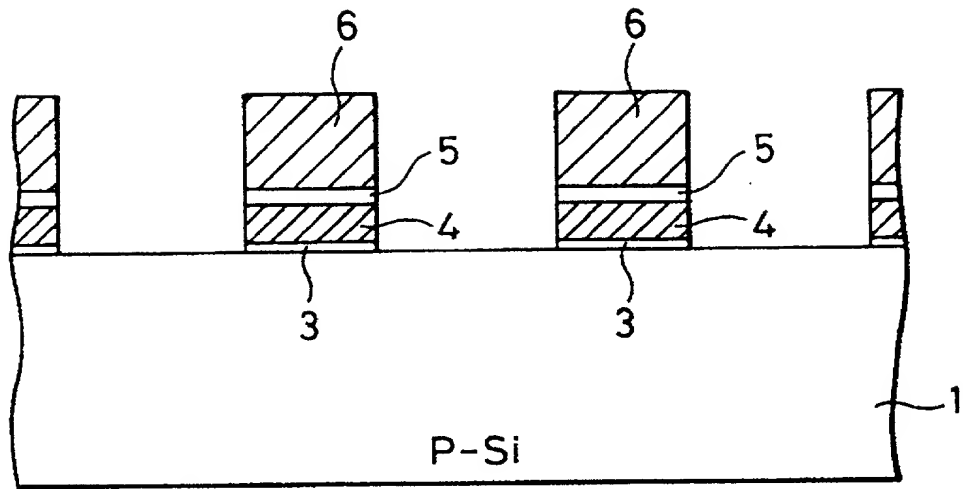


FIG. 4 (a)

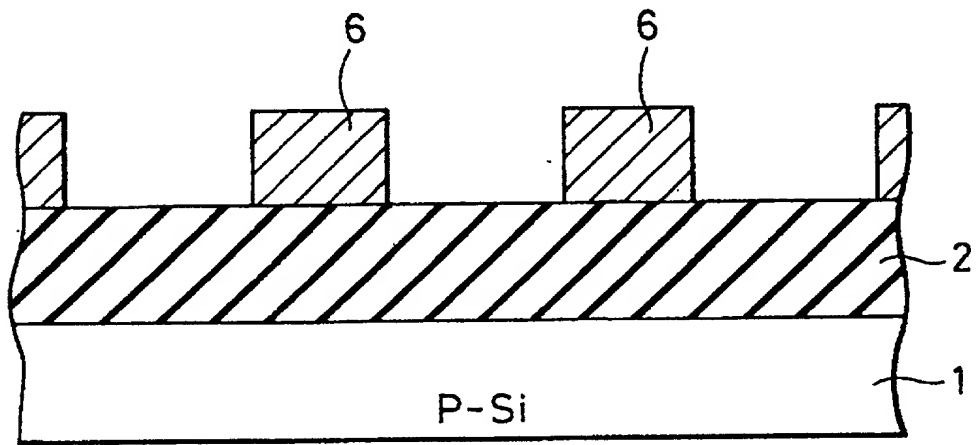


FIG. 4 (b)



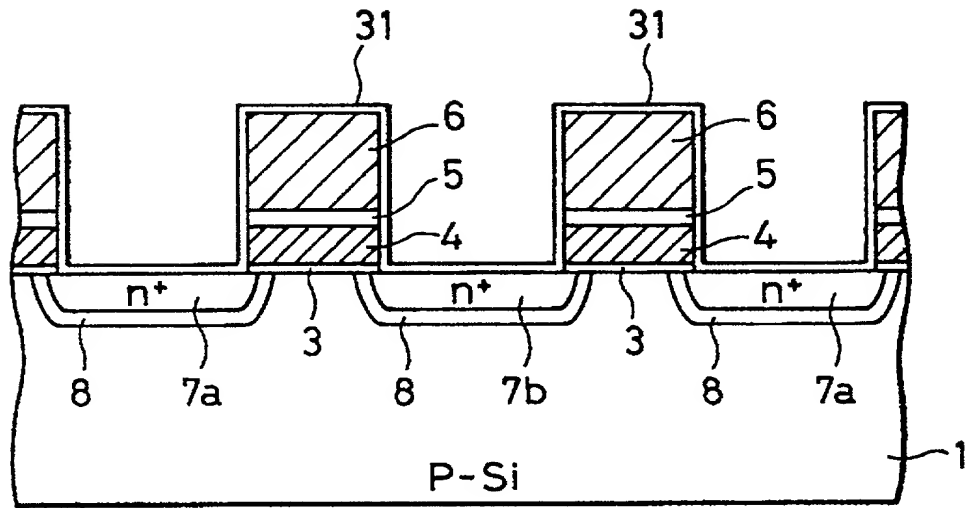


FIG. 5 (a)

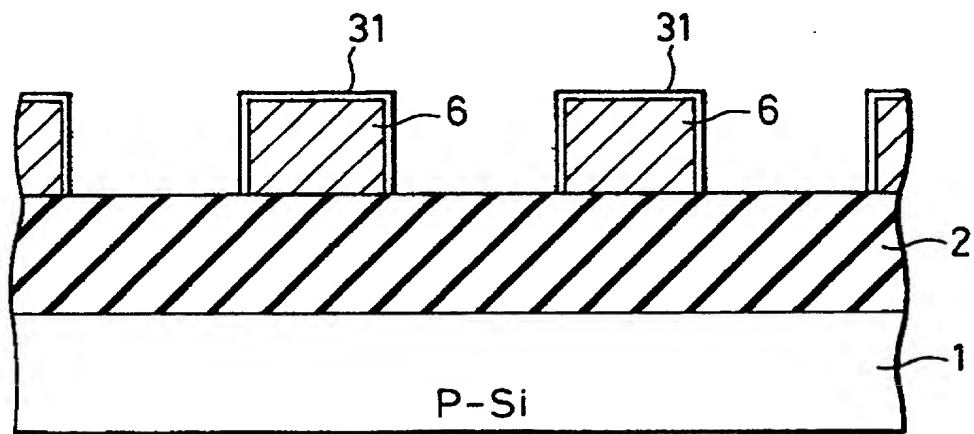


FIG. 5 (b)

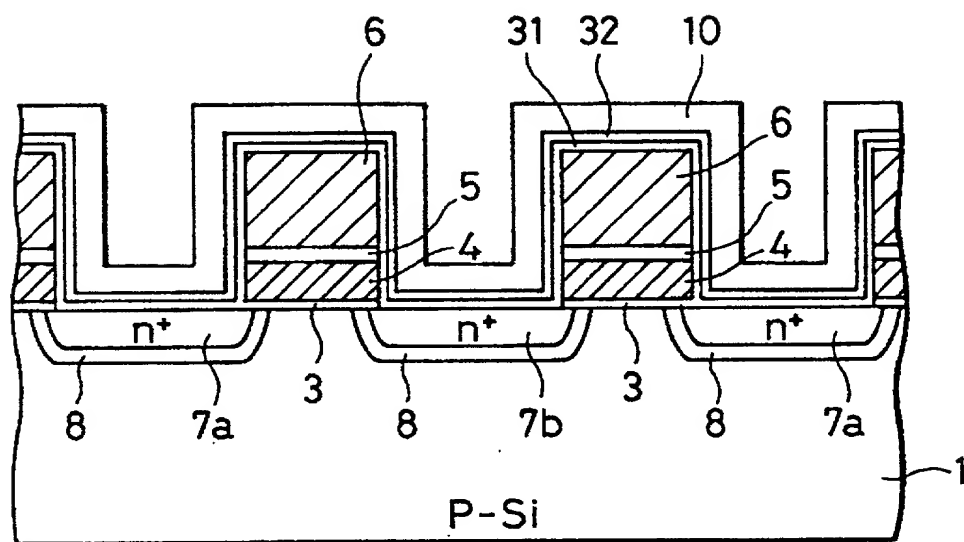


FIG. 6 (a)

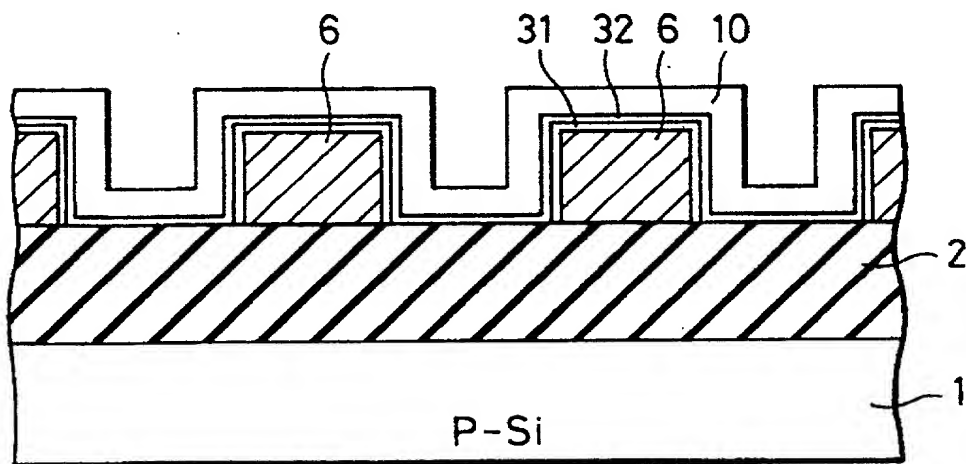


FIG. 6 (b)

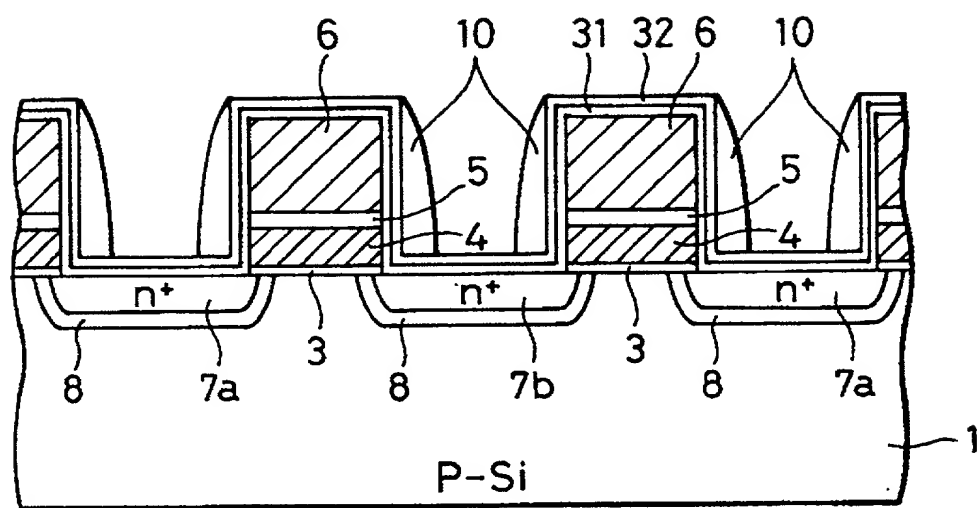


FIG. 7 (a)

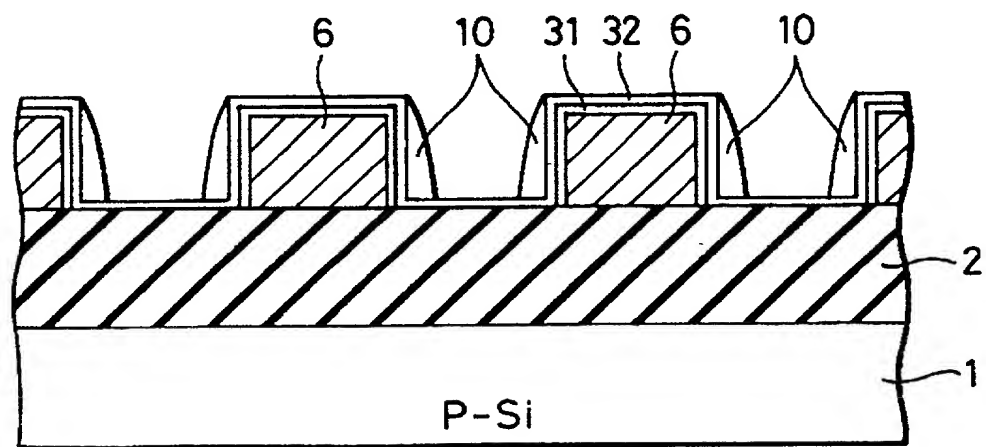


FIG. 7 (b)

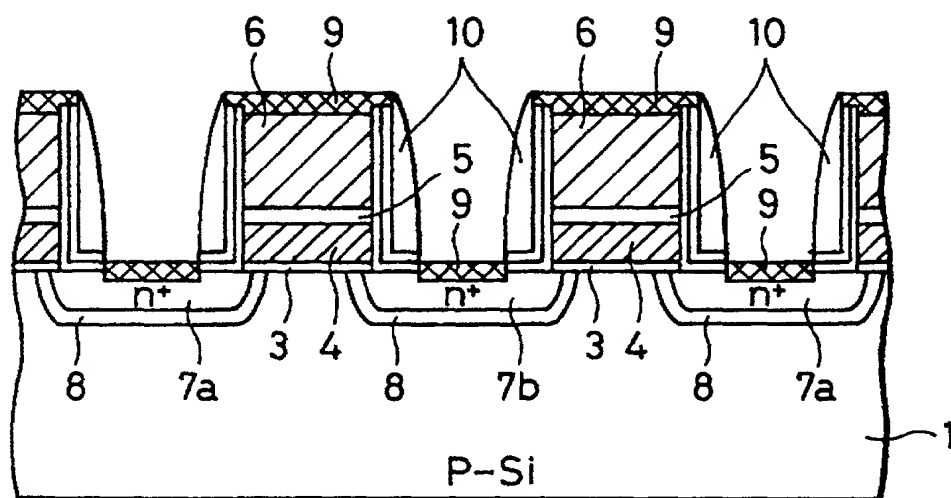


FIG. 8 (a)

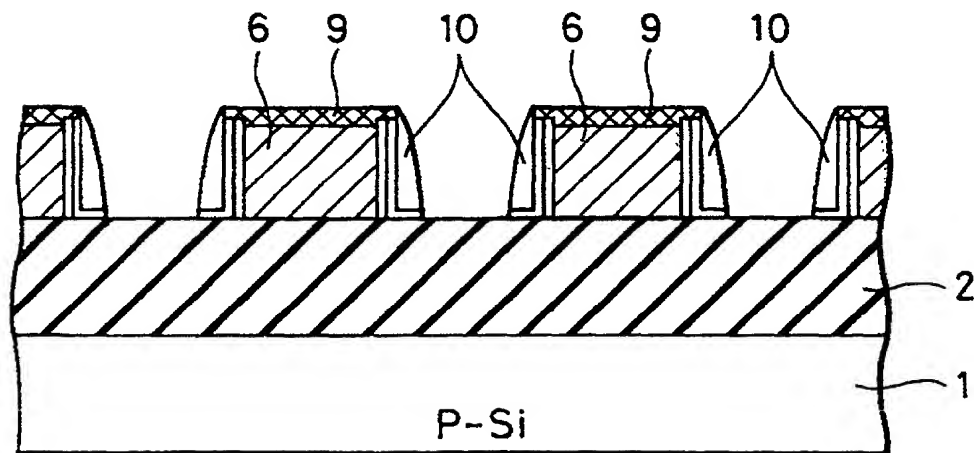


FIG. 8 (b)

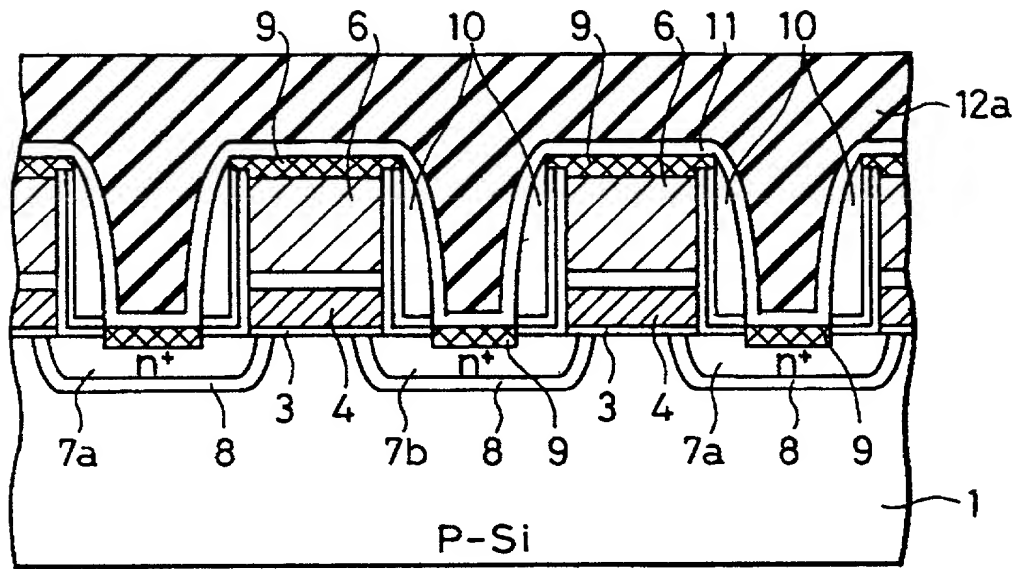


FIG. 9 (a)

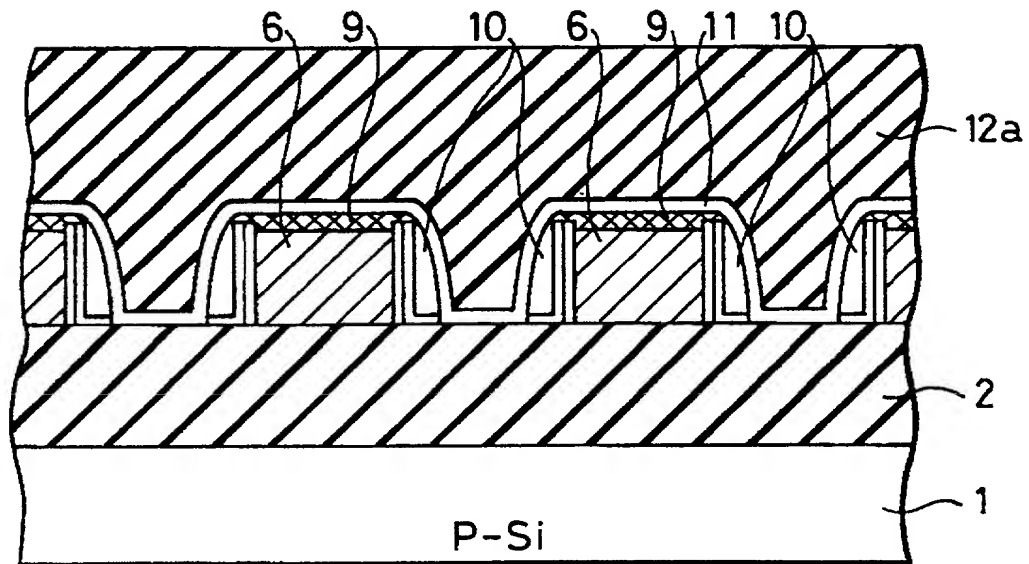


FIG. 9 (b)

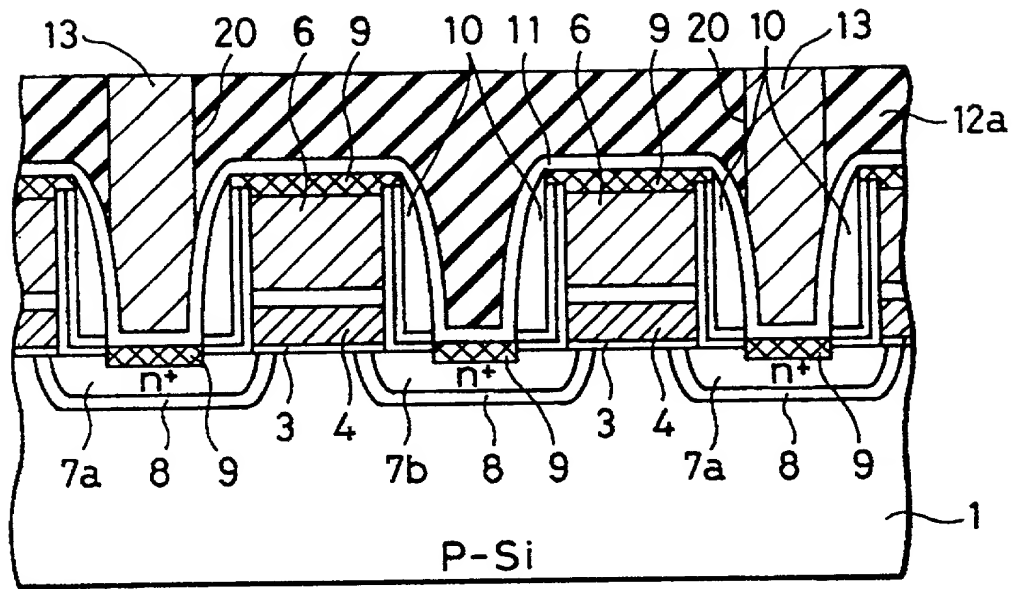


FIG. 10 (a)

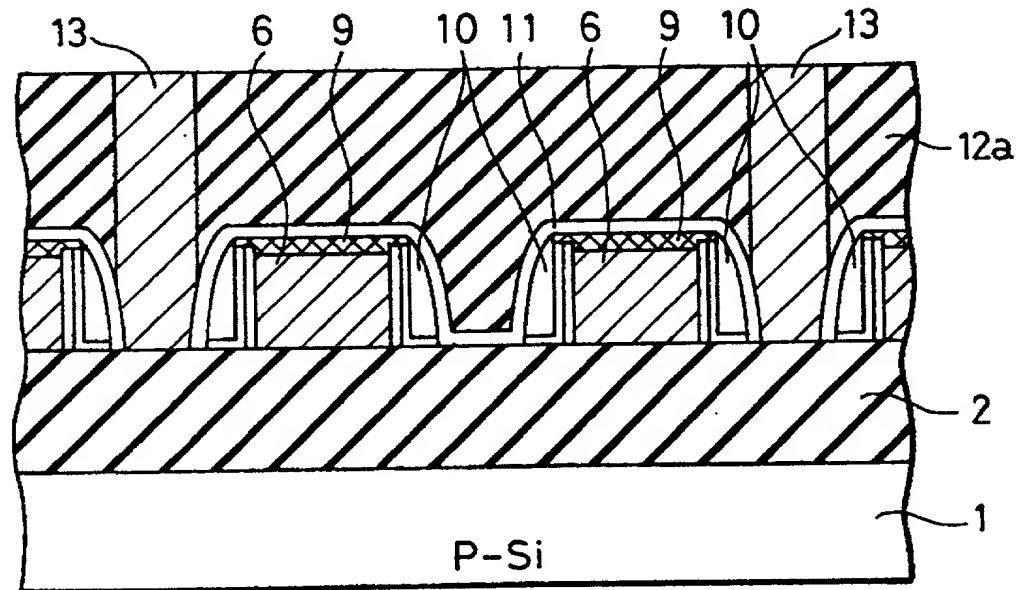


FIG. 10 (b)

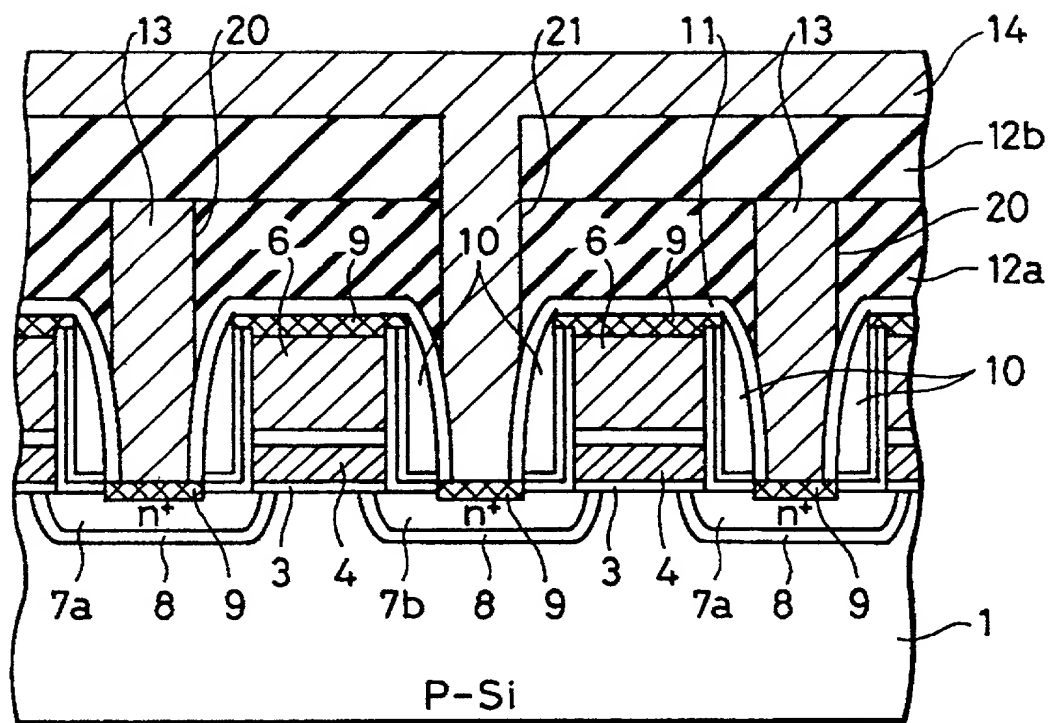


FIG. 11 (a)

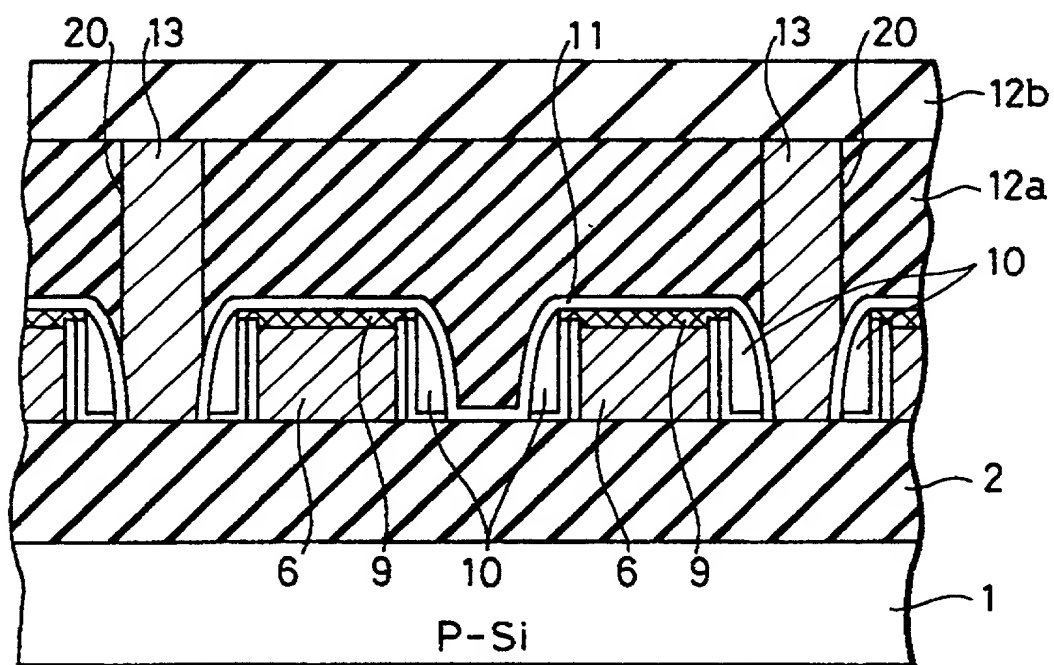
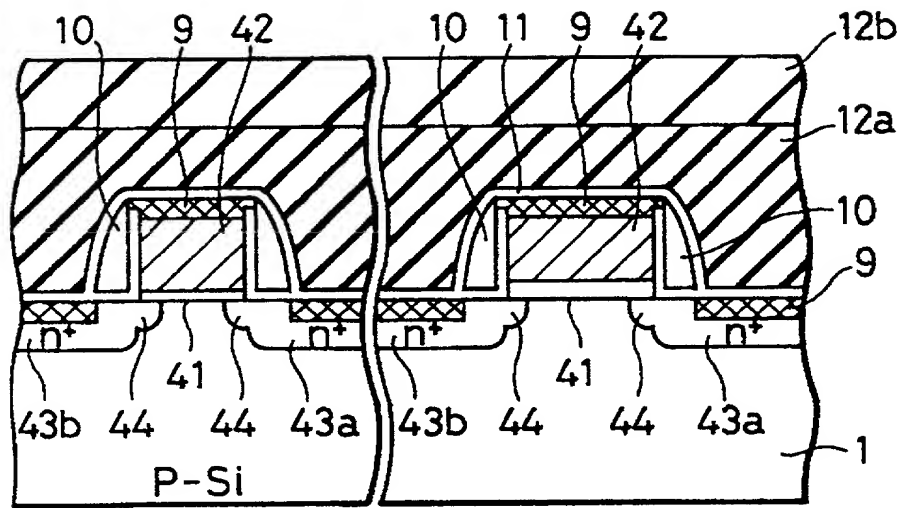


FIG. 11 (b)



[LOW-VOLTAGE MOS]

[HIGH-VOLTAGE MOS]

FIG. 12



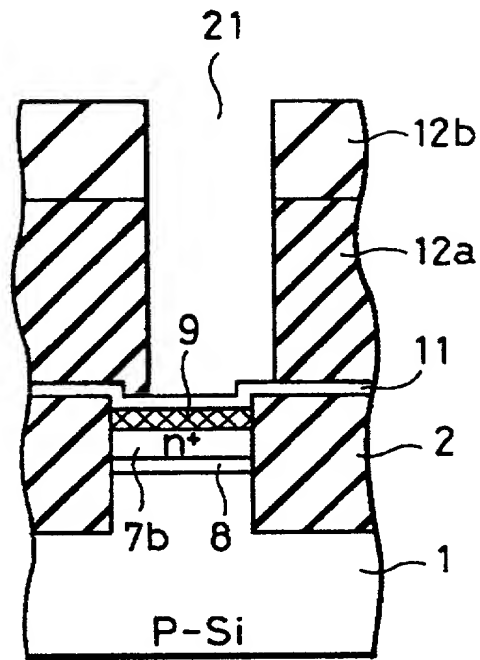


FIG. 13

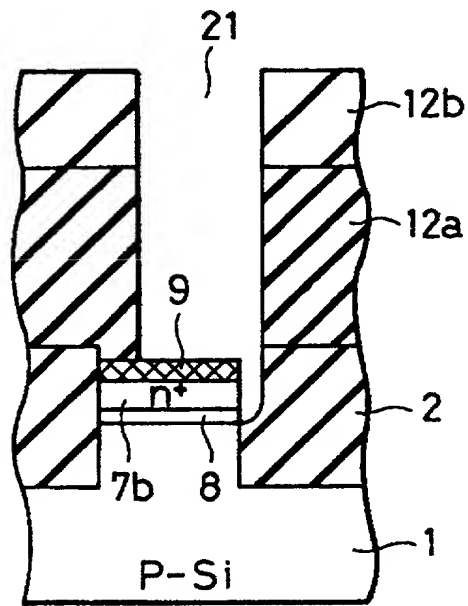
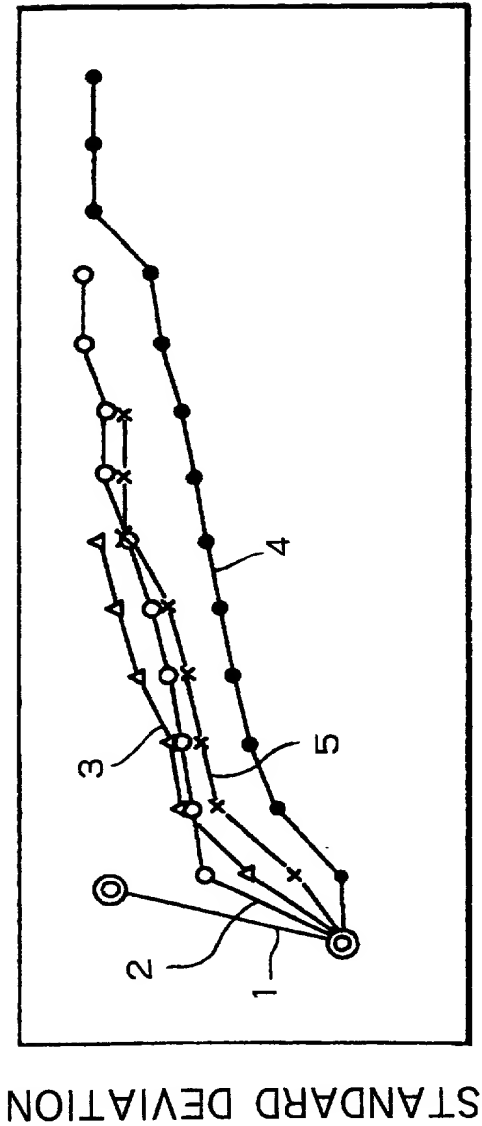


FIG. 14



THRESHOLD VALUE  $V_{th}$

- 1 : INITIAL VALUE
  - 2 : COMPARATIVE EXAMPLE 1
  - 3 : COMPARATIVE EXAMPLE 2
  - 4 : COMPARATIVE EXAMPLE 3
  - 5 : EMBODIMENT OF THE PRESENT INVENTION
- SIDE WALL  $\text{SiO}_2$
  - △ SIDE WALL  $\text{SiN}$
  - SIDE WALL  $\text{SiO}_2 + \text{P.SiN}$
  - × SIDE WALL  $\text{SiN} + \text{P.SiN}$

FIG. 15